

MATLAB EXPO 2019

Wired Communications Systems Modeling and Analysis

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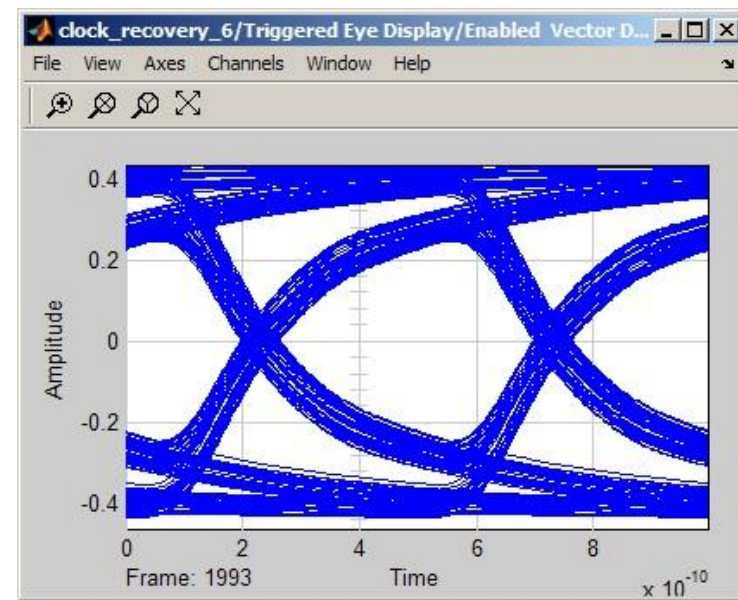
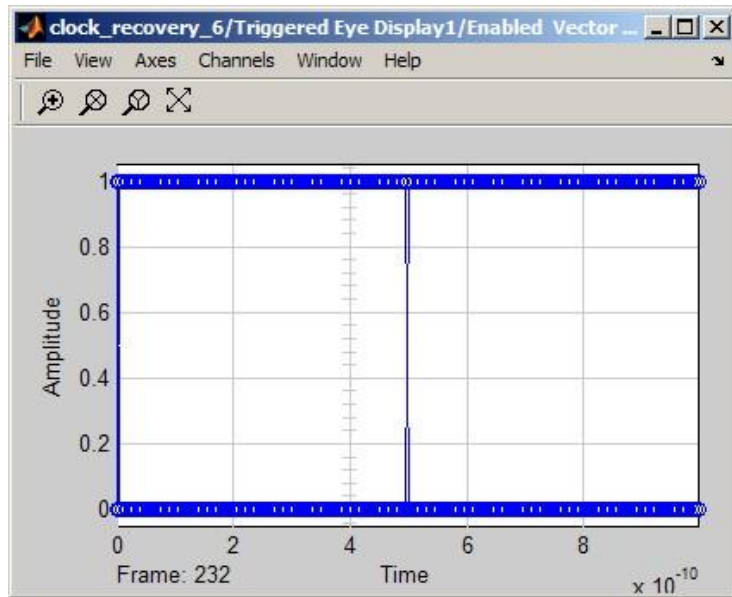


What's Covered

- Introduction to SerDes Design and Signal Integrity Analysis
- Using SerDes Toolbox for System-Level Design and Analysis
- Automatic Generation of Standard Compliant IBIS-AMI Models
- SerDes Verification Using Channel Simulators

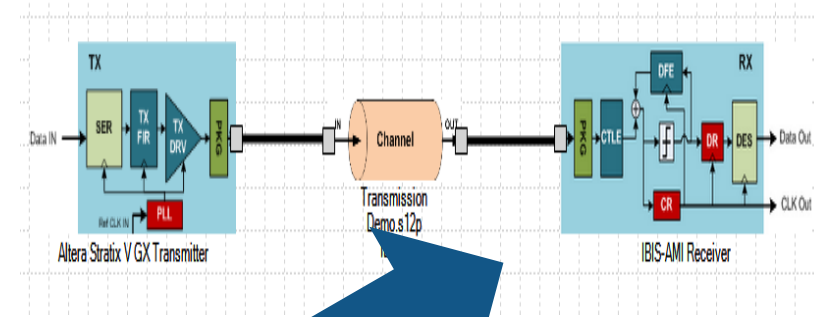
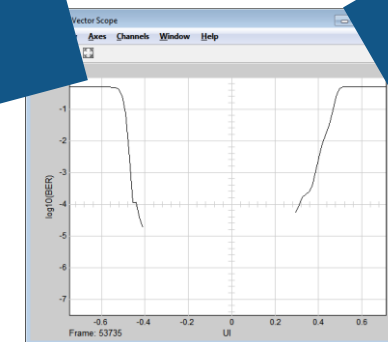
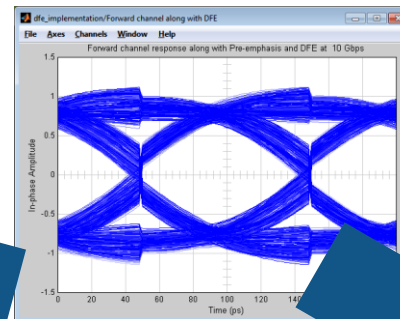
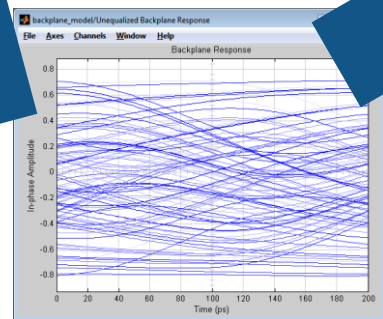
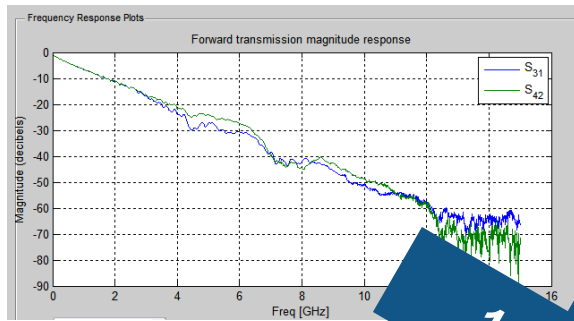
Introduction to SerDes Design and Signal Integrity Analysis

What is Signal Integrity?

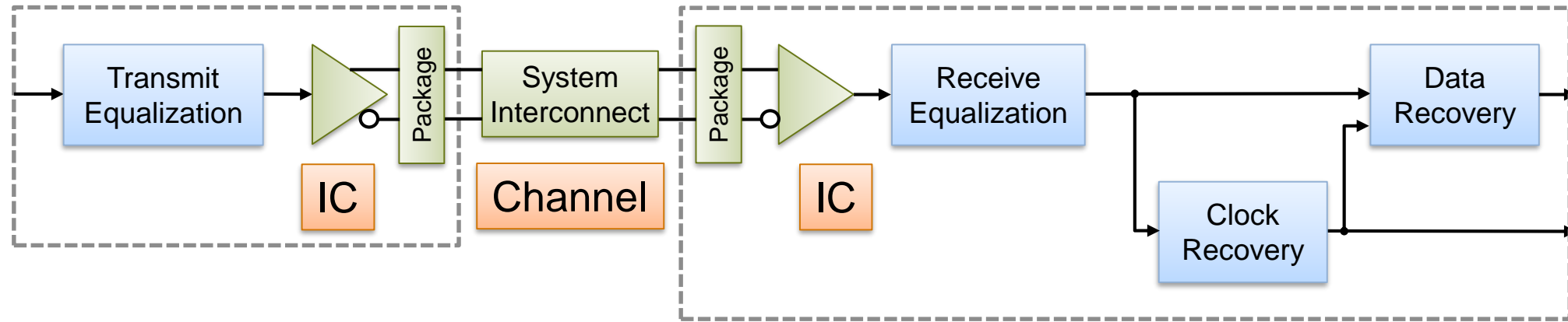


Typical SerDes Design Workflow

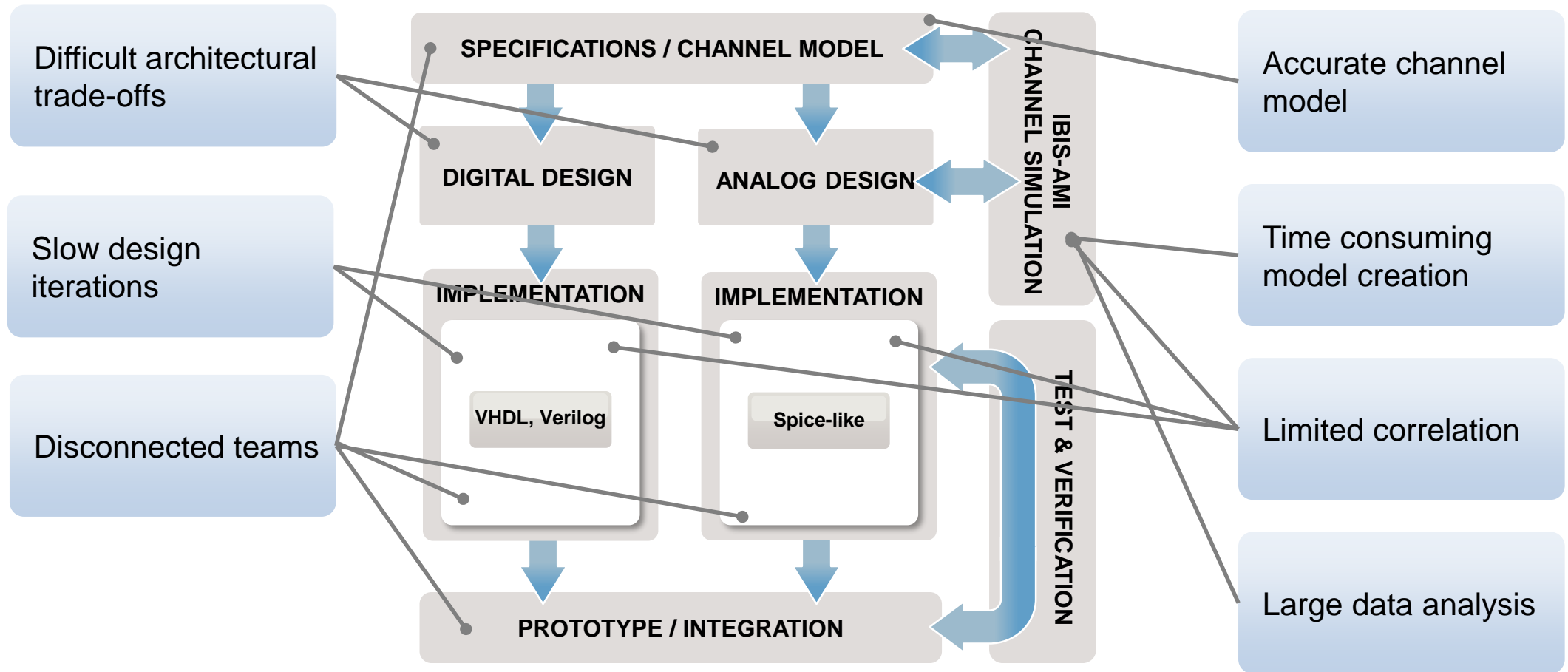
1. Time-domain characterization of the channel
2. Design of analog and digital equalizers
3. Simulation of the system performance in the time domain
4. Hardware implementation and IP verification
5. IBIS-AMI model generation and SerDes system verification



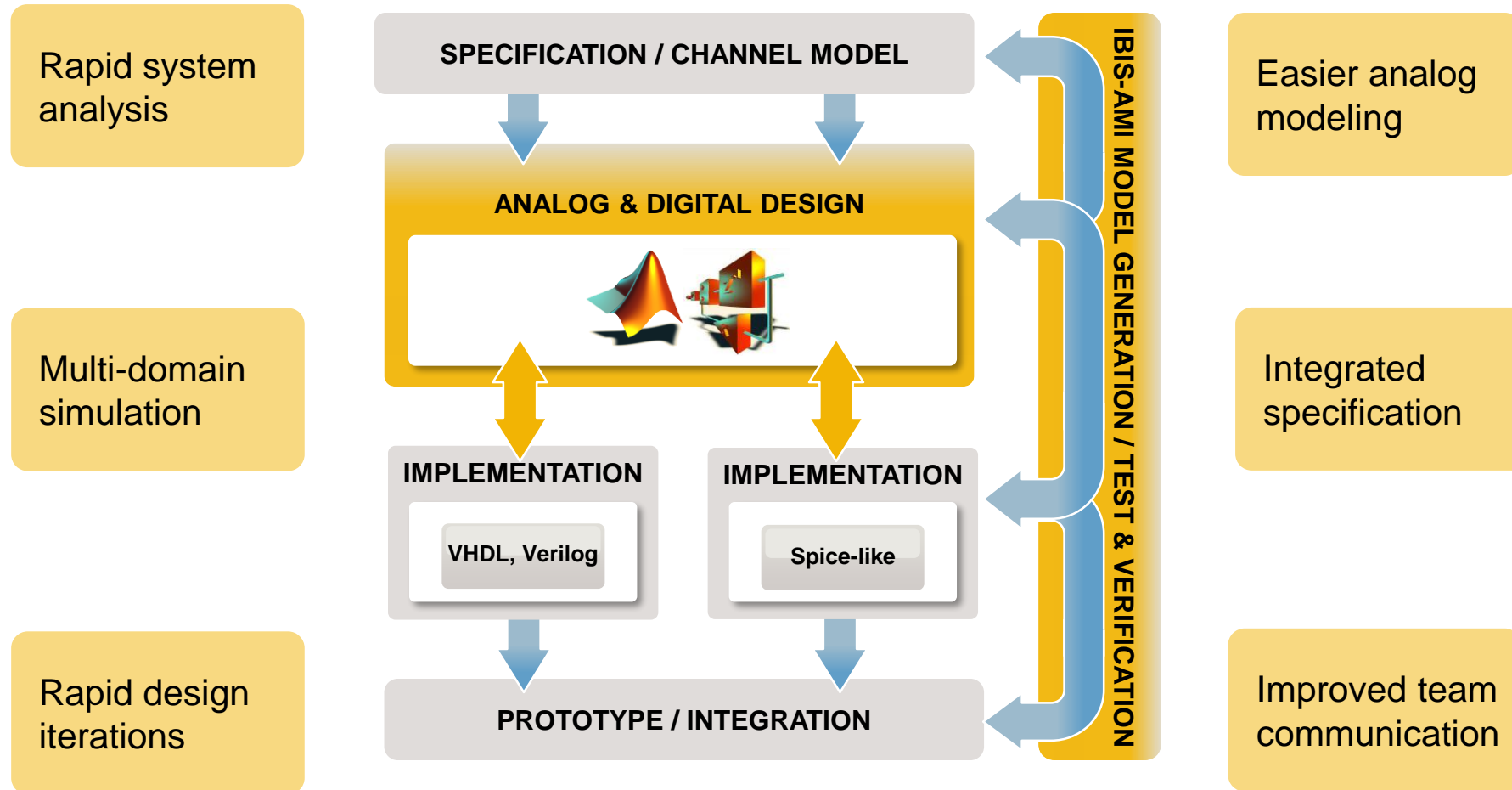
A Typical SerDes System: TX, RX, and Channel



SerDes Design and Verification Challenges

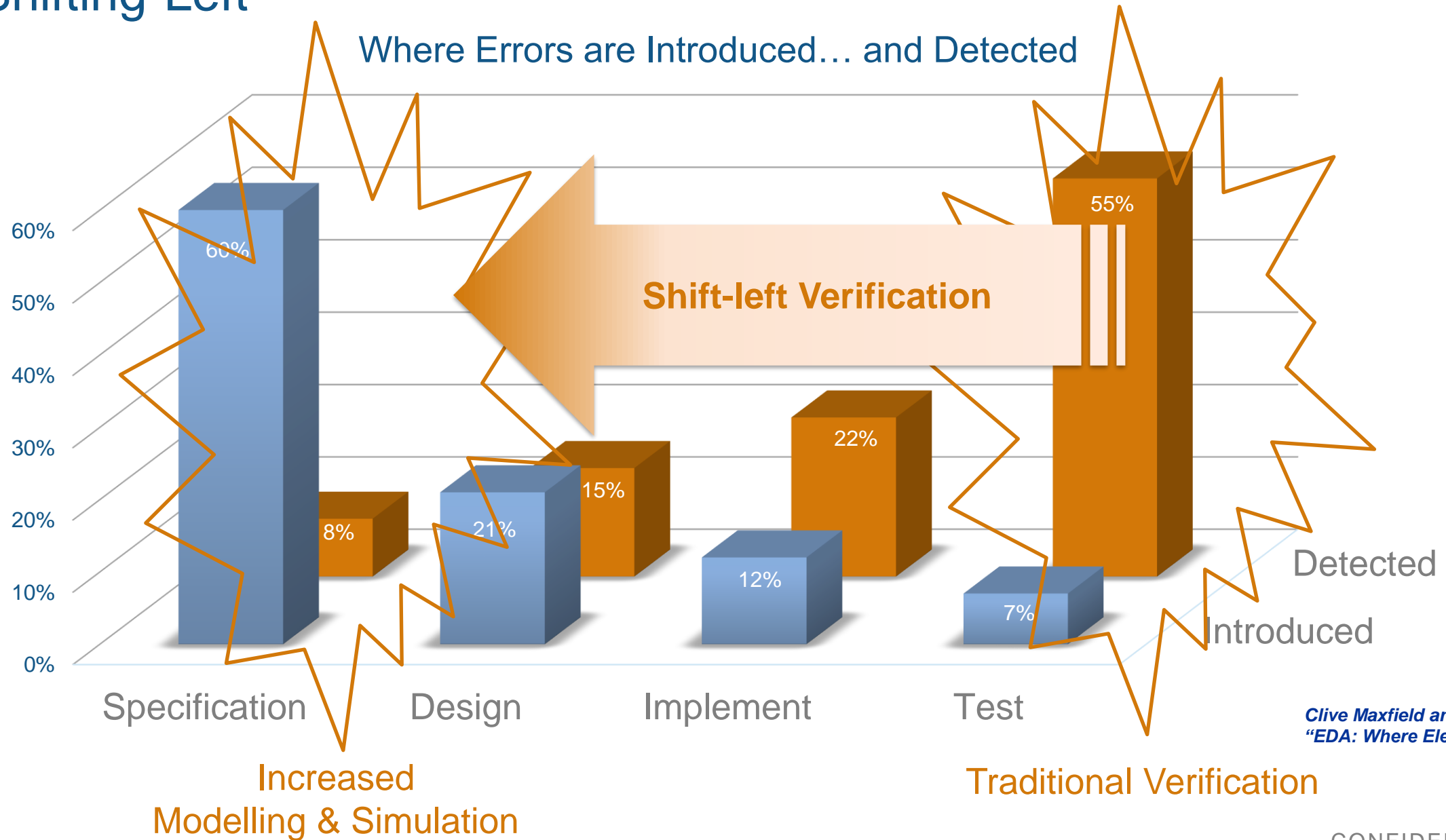


System-Level Design and Analysis Leads to Continuous Verification



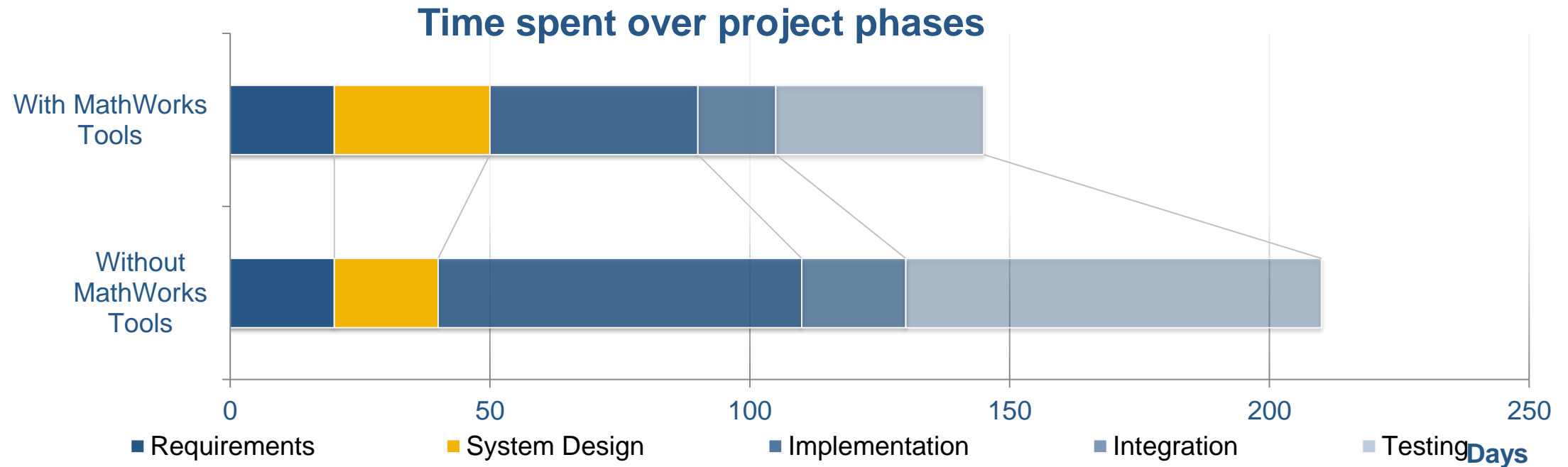
Shifting-Left

Where Errors are Introduced... and Detected



Clive Maxfield and Kuhoo Goyal
"EDA: Where Electronics Begins"

Save 30% of Overall Development Time (and improve quality, reduce re-spins, etc.)



EE Times - Top-down verification guides mixed-signal designs

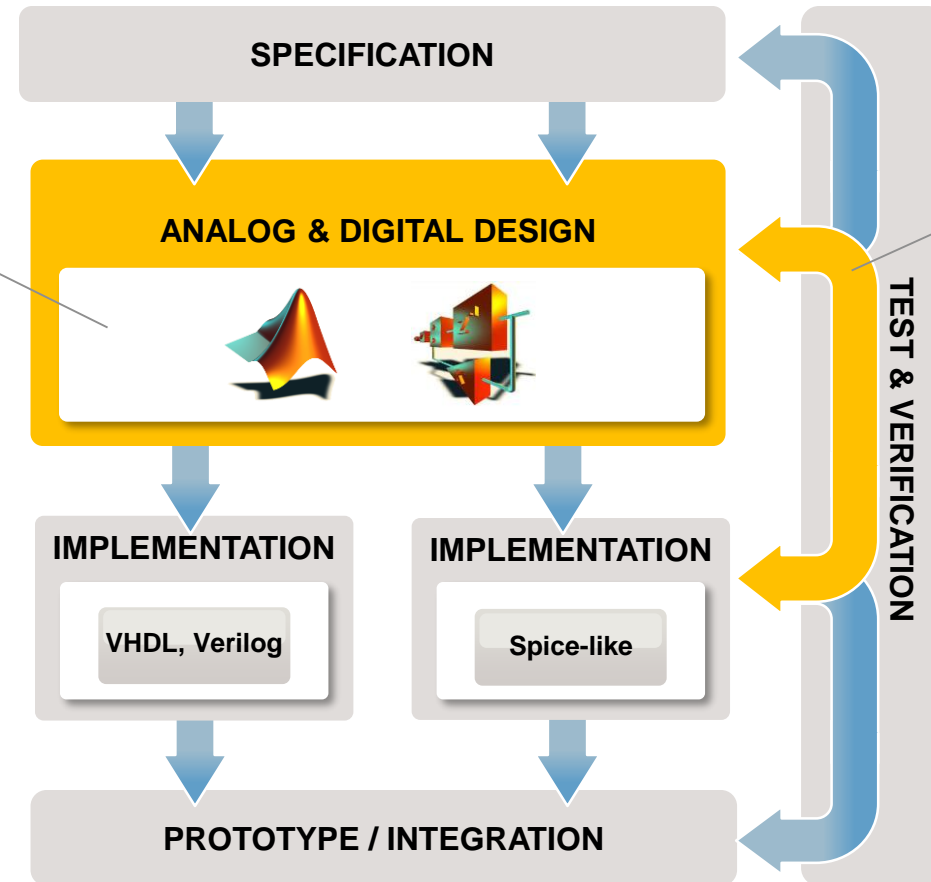
[K. Kundert and H. Chang, Partners, Designer's Guide Consulting](#)

*“In order to address these challenges, many design teams are either looking to, or else have already implemented, a **top-down design methodology**. In a top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as **MATLAB or Simulink**. From the high-level simulation, requirements for the individual circuit blocks are derived.”*

What's New

R2019a

SerDes Toolbox

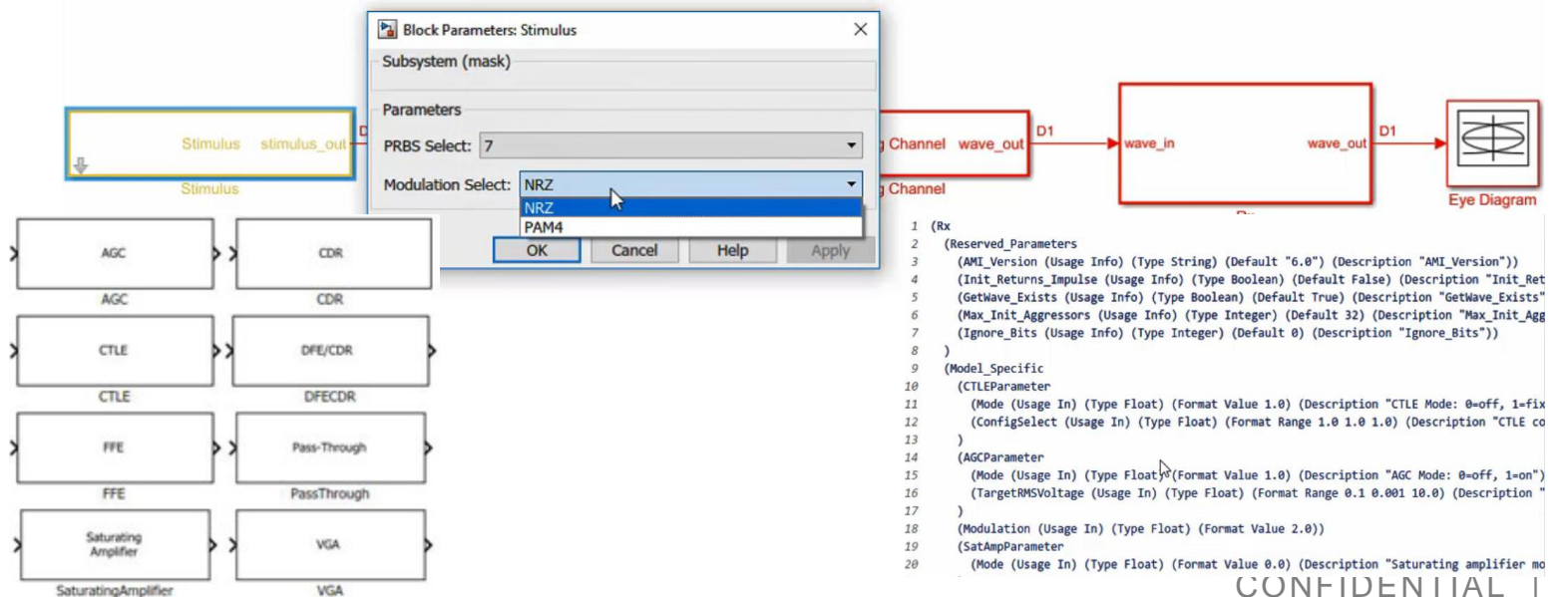
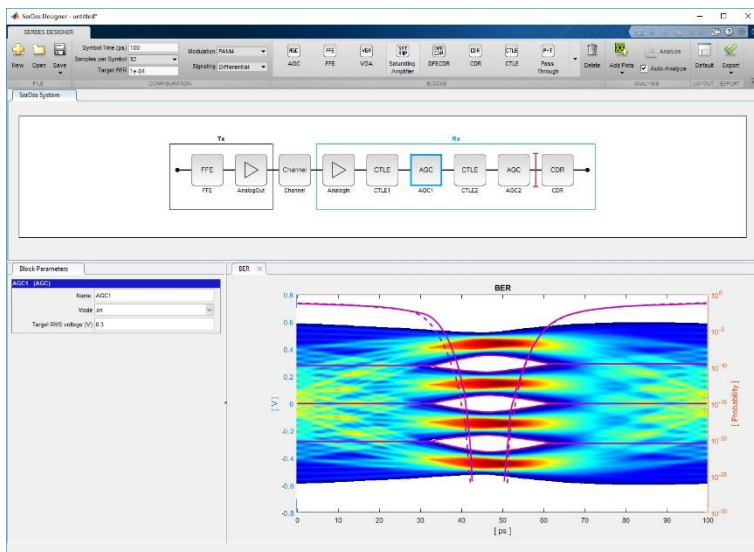


Integration with IC design tools and **channel simulators**

R2019a SerDes Toolbox

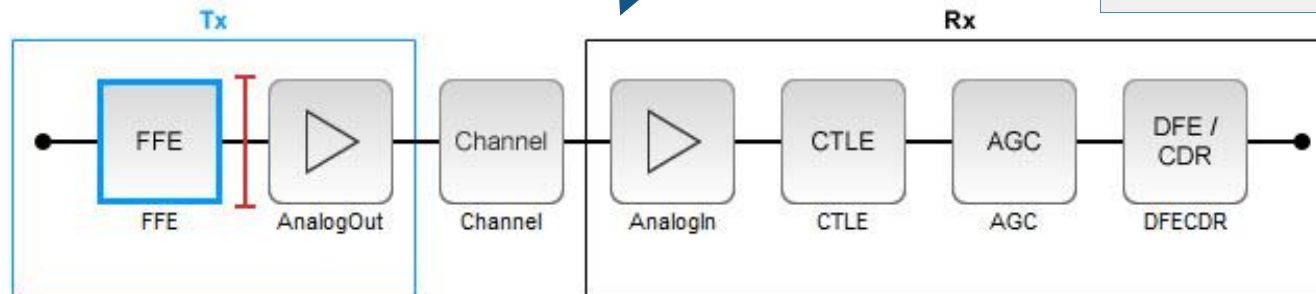
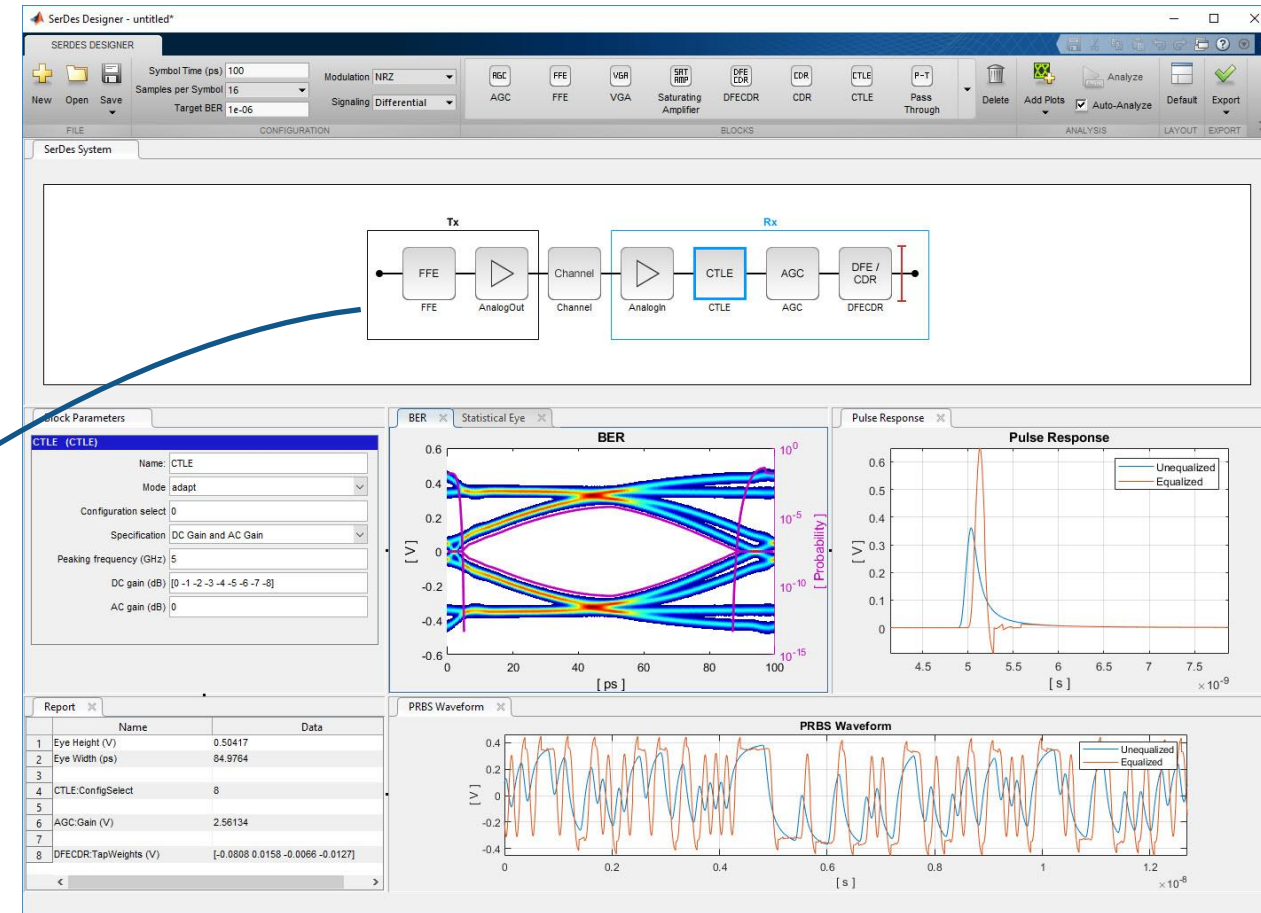
Design SerDes systems and generate IBIS-AMI models for high-speed digital interconnects

- Design and analyze transmitters and receivers with the SerDes Designer app
- Develop equalization algorithms with MATLAB System objects and Simulink blocks
 - FFE, DFE, AGC, CDR, CTLE, etc...
- Perform SerDes statistical analysis and time-domain simulation
- Generate dual IBIS-AMI models for 3rd party channel simulators
- Use reference designs for high-speed links such as Ethernet CEI-56G, DDR5, PCI-Gen4, USB3.1



SerDes Designer app: No Need to be a SerDes Expert

- Design and analyze SerDes systems including transmitters and receivers with arbitrary configuration
- Use parameterized building blocks
- Perform statistical analysis: eye diagram, BER, bathtub, pulse response....



SerDes Design: Where to Start?

Add SerDes components

- Export to:
- MATLAB
 - Simulink
 - IBIS-AMI

- Modulation
- Sample rate
- Signaling

The screenshot shows the SerDes Designer software interface. At the top, the configuration panel includes fields for Symbol Time (ps) set to 100, Samples per Symbol set to 16, and Target BER set to 1e-06. A toolbar contains various SerDes components like AGC, FFE, VGR, SRT AMP, DFECDR, CDR, CTLE, and P-T. A central block diagram shows a Tx path (FFE, AnalogOut, Channel) and an Rx path (AnalogIn, CTLE, AGC, DFECDR). Below the diagram, the Block Parameters panel for the CTLE block is shown, with fields for Name, Mode, Specification, Peaking frequency, DC gain, and AC gain. To the right, three plots are displayed: BER (Bit Error Rate) vs. time, Pulse Response (Voltage vs. time) comparing Unequalized and Equalized signals, and PRBS Waveform (Voltage vs. time) also comparing Unequalized and Equalized signals. A Report table is visible at the bottom left.

Report	Name	Data
1	Eye Height (V)	0.50417
2	Eye Width (ps)	84.9764
3		
4	CTLE:ConfigSelect	8
5		
6	AGC:Gain (V)	2.56134
7		
8	DFECDR:TapWeights (V)	[-0.0808 0.0158 -0.0066 -0.0127]

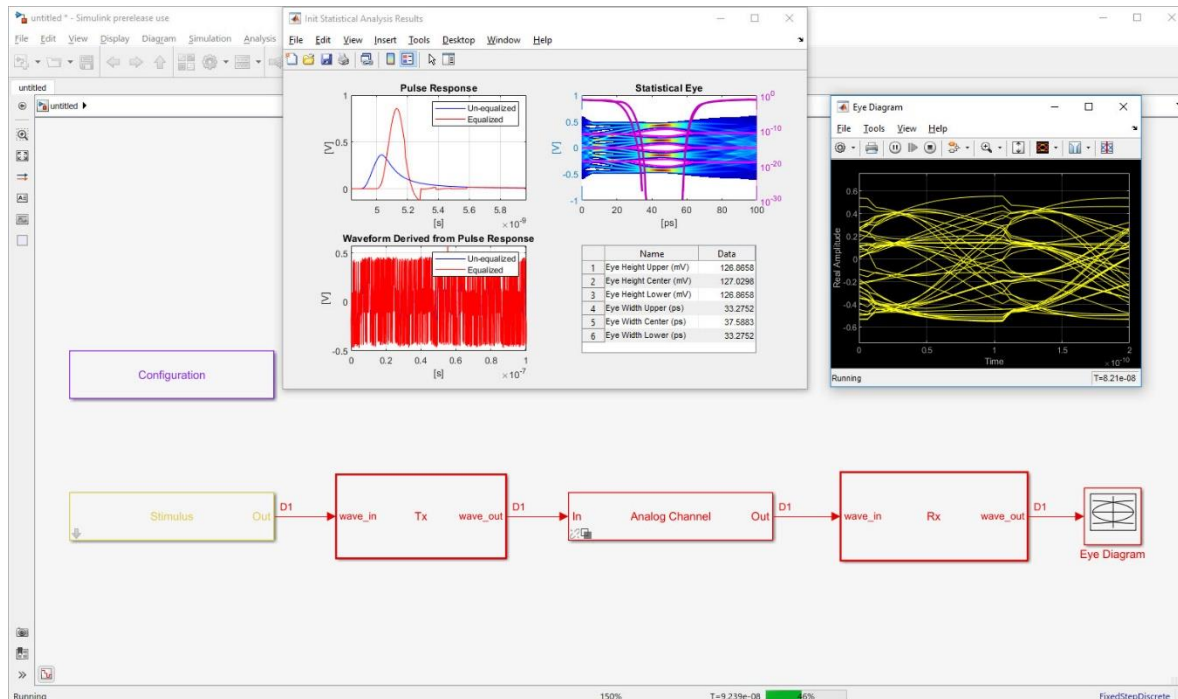
Plot analysis results

High-speed link

Component specifications

SerDes Top Down Design

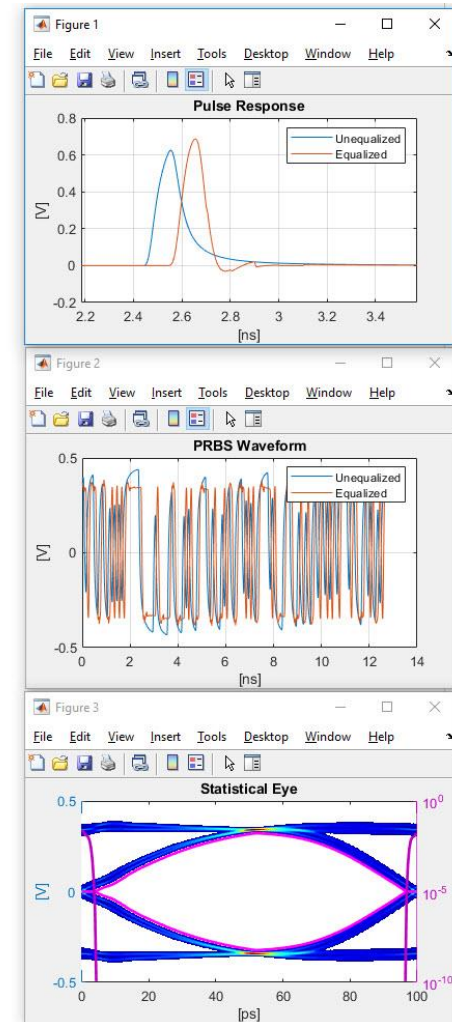
- Create a MATLAB script for automation and design space exploration
- Export to Simulink models for time-domain simulation
- Create dual IBIS-AMI models



```

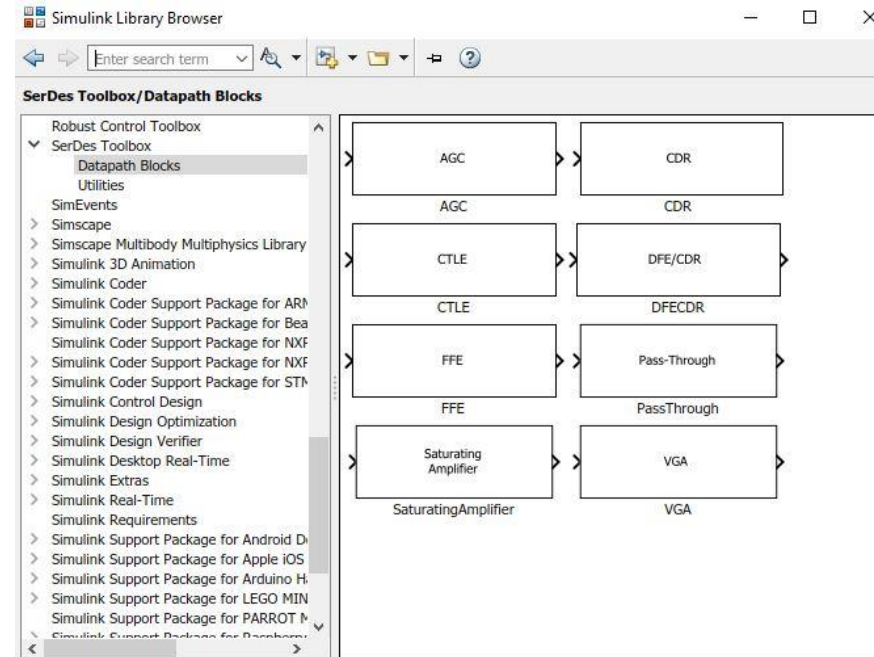
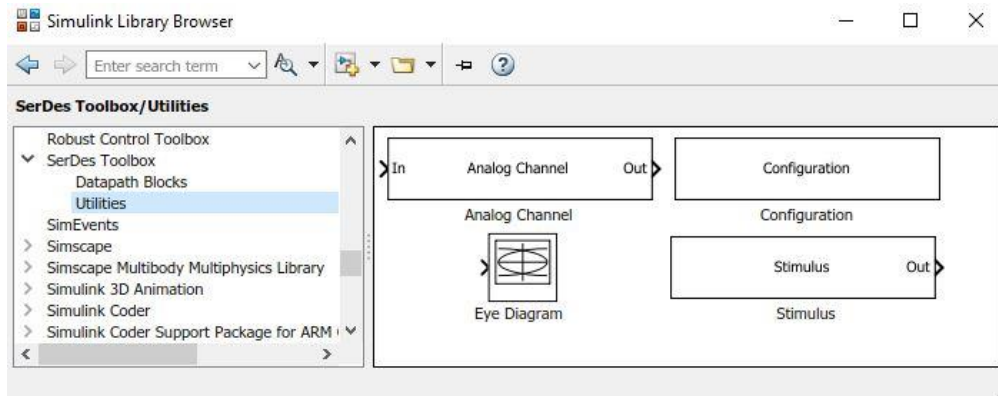
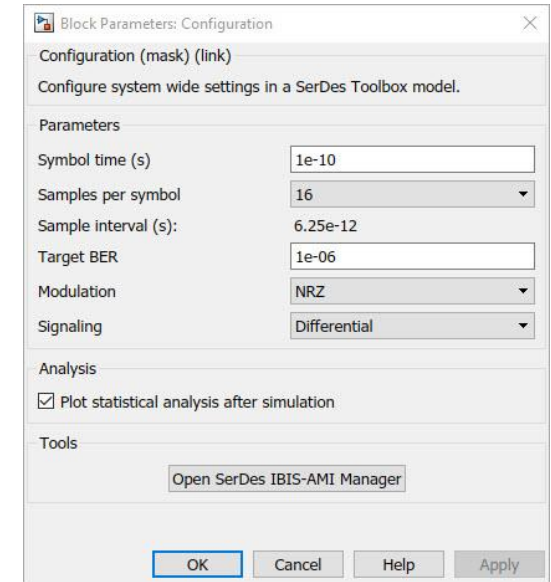
1  %-----
2  % MATLAB script to build SerDes System
3  %-----
4
5  % Build cell array of Tx blocks:
6  txBlocks(1) = serdes.FFE;
7  txBlocks(1).BlockName = 'FFE';
8  txBlocks(1).Mode = 1;
9  txBlocks(1).TapWeights = [0 1 0 0 0];
10 txBlocks(1).Normalize = true;
11
12
13 % Build cell array of Rx blocks:
14 rxBlocks(1) = serdes.CTLE;
15 rxBlocks(1).BlockName = 'CTLE';
16 rxBlocks(1).Mode = 2;
17 rxBlocks(1).ConfigSelect = 0;
18 rxBlocks(1).Specification = 'DC Gain and Peaking Gain';
19 rxBlocks(1).PeakingFrequency = 5000000000;
20 rxBlocks(1).DCGain = [0 -1 -2 -3 -4 -5 -6 -7 -8];
21 rxBlocks(1).PeakingGain = [0 1 2 3 4 5 6 7 8];
22
23
24 rxBlocks(2) = serdes.AGC;
25 rxBlocks(2).BlockName = 'AGC';
26 rxBlocks(2).Mode = 1;
27 rxBlocks(2).TargetRMSVoltage = 0.3;
28
29
30 rxBlocks(3) = serdes.DFECDR;
31 rxBlocks(3).BlockName = 'DFECDR';
32 rxBlocks(3).Mode = 2;
33 rxBlocks(3).TapWeights = [0 0 0 0];
34 rxBlocks(3).MinimumTap = -1;
35 rxBlocks(3).MaximumTap = 1;
36
37 % Build txModel:
38 txAnalogModel = AnalogModel( ...
39     'R',50, ...
40     'C',1.000000e-13);
41 tx = Transmitter( ...
42     'Blocks',txBlocks, ...
43     'AnalogModel',txAnalogModel, ...
44     'RiseTime',1.000000e-11, ...
45     'VoltageSwingIdeal',1, ...
46     'Name','TX');
47
48 % Build rxModel:
49 rxAnalogModel = AnalogModel( ...
50     'R',50, ...
51     'C',2.000000e-13);
52 rx = Receiver( ...
53     'Blocks',rxBlocks, ...
54     'AnalogModel',rxAnalogModel, ...
55     'Name','RX');
56
57 % Build ChannelData:
58 channel = ChannelData( ...
59     'ChannelLossB',8, ...
60     'ChannelLossFreq',5000000000, ...
61     'ChannelDifferentialImpedance',100);
62
63 % Build SerDes System:
64 SymbolTime = 1e-10;
65 SamplesPerSymbol = 16;
66 ModulationLevels = 2;
67 BERtarget = 1e-06;

```



SerDes Toolbox: Simulink Models

- Develop adaptive equalizers using white-box models such as DFE, CTLE, AGC, and CDR
- Use parametrized blocks and algorithms for single-ended and differential signals
- Generate PRBS and custom stimulus patterns supporting PAM4 and NRZ modulation



SerDes Simulation and Architecture Exploration

Configuration



Global Parameters

The screenshot shows the 'Global Parameters' window in the SerDes IBIS-AMI Manager. The 'Node Details' for 'PAM4_UpperThreshold' are visible, including its description, type (Float), usage (Out), format (Value), and current value (0.333).

Channel modeling

Block Parameters: Analog Channel

AnalogChannel (mask) (link)

Construct loss model using a channel loss metric or an impulse response from another source in a SerDes Toolbox model. Analog model inputs are only used for IBIS file construction when using impulse response.

Channel Model

Channel model: Impulse response

Impulse response: `[zeros(1,63),1/SampleInterval,zeros(1,192)]`

Analog Model

Tx R (Ohms): 50, Tx C (F): 160e-15, Rx R (Ohms): 50, Rx C (F): 160e-15, Rise time (s): 2.905e-12, Voltage (V): 1

Buttons: OK, Cancel, Help, Apply

White-box (customizable) models

%Note that step or time domain adaptation of the CTLE must be %done in an exterior block.

```

fixed(obj)
= obj.ConfigSelect;|
privConfigInitialFlag
obj.privConfigInitial = obj.ConfigSelect;
obj.privConfigInitialFlag = false;
obj.privConfigInitial = obj.ConfigSelect;
= obj.privConfigInitial;
obj.FilterCoefficients.np(Config+1)+1;
obj.FilterCoefficients.nz(Config+1)+1;
    
```

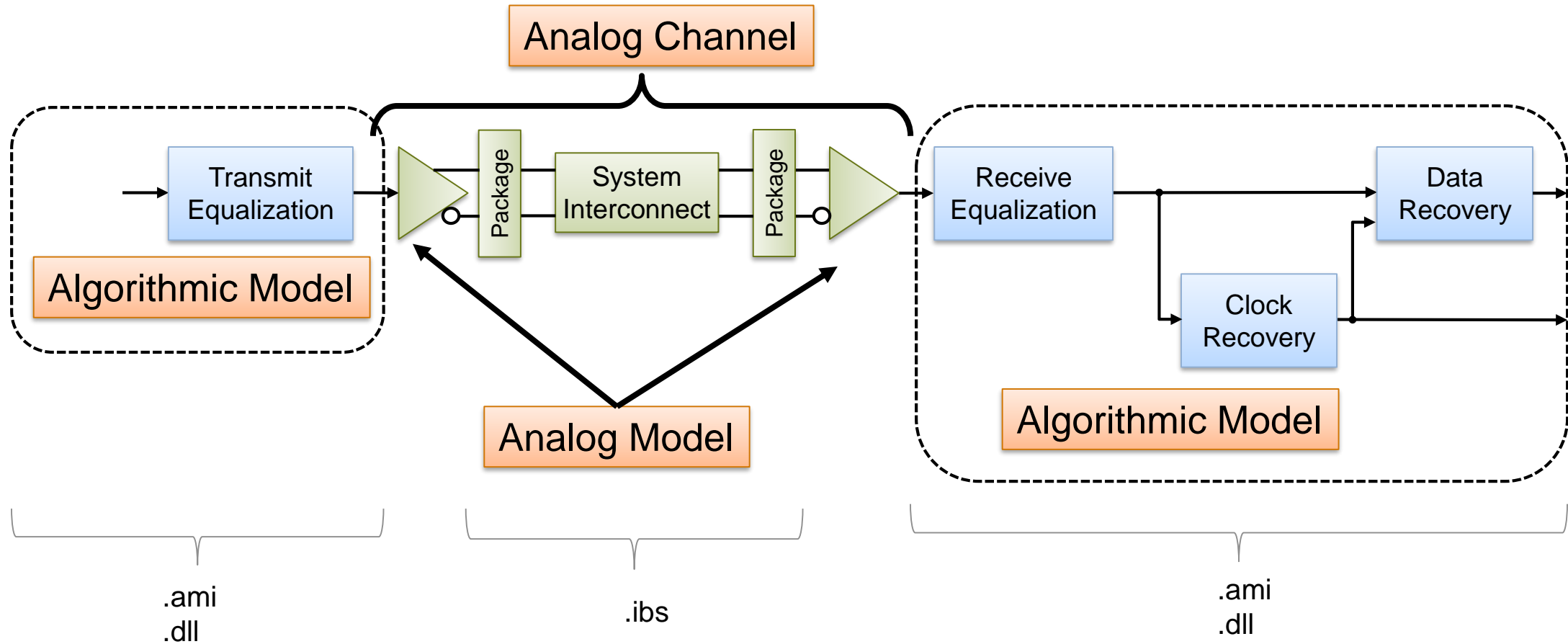
Simulate and customize adaptive equalizers

The diagram shows a CTLE block with the following inputs and outputs:

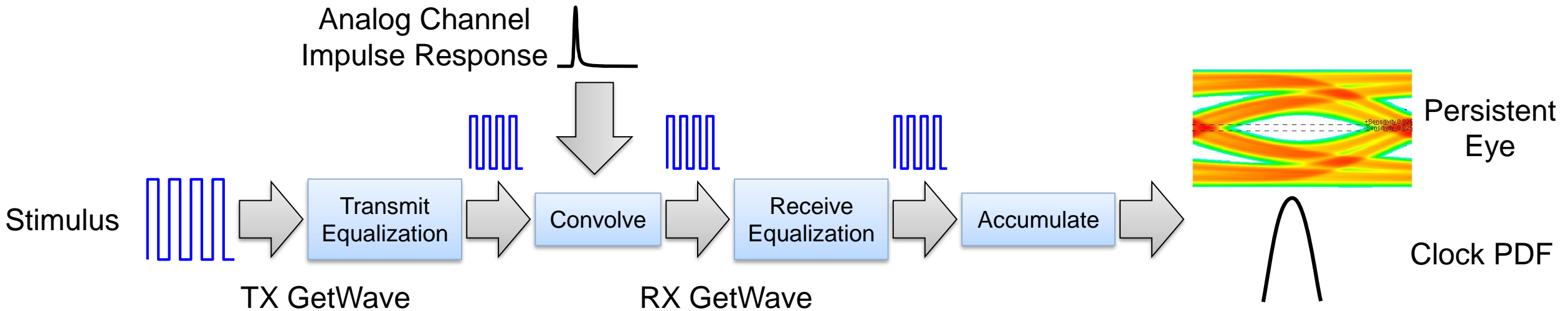
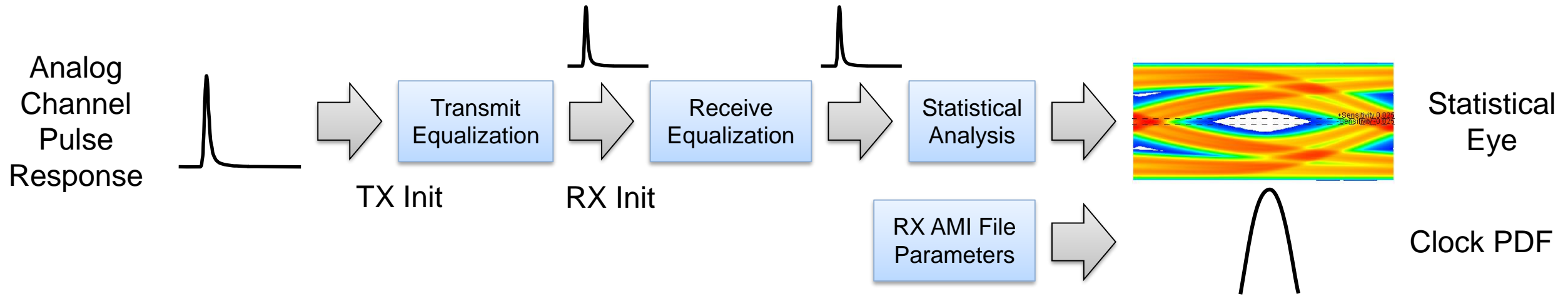
- Input: D1 (labeled 1)
- Input: Mode (from CTLEParameter.Mode)
- Input: ConfigSelect (from CTLESignal.ConfigSelect)
- Output: D1 (labeled 1)
- Output: ConfigSelect (to CTLESignal.ConfigSelect)

Automatic Generation of Standard Compliant IBIS-AMI Models

IBIS-AMI Terminology

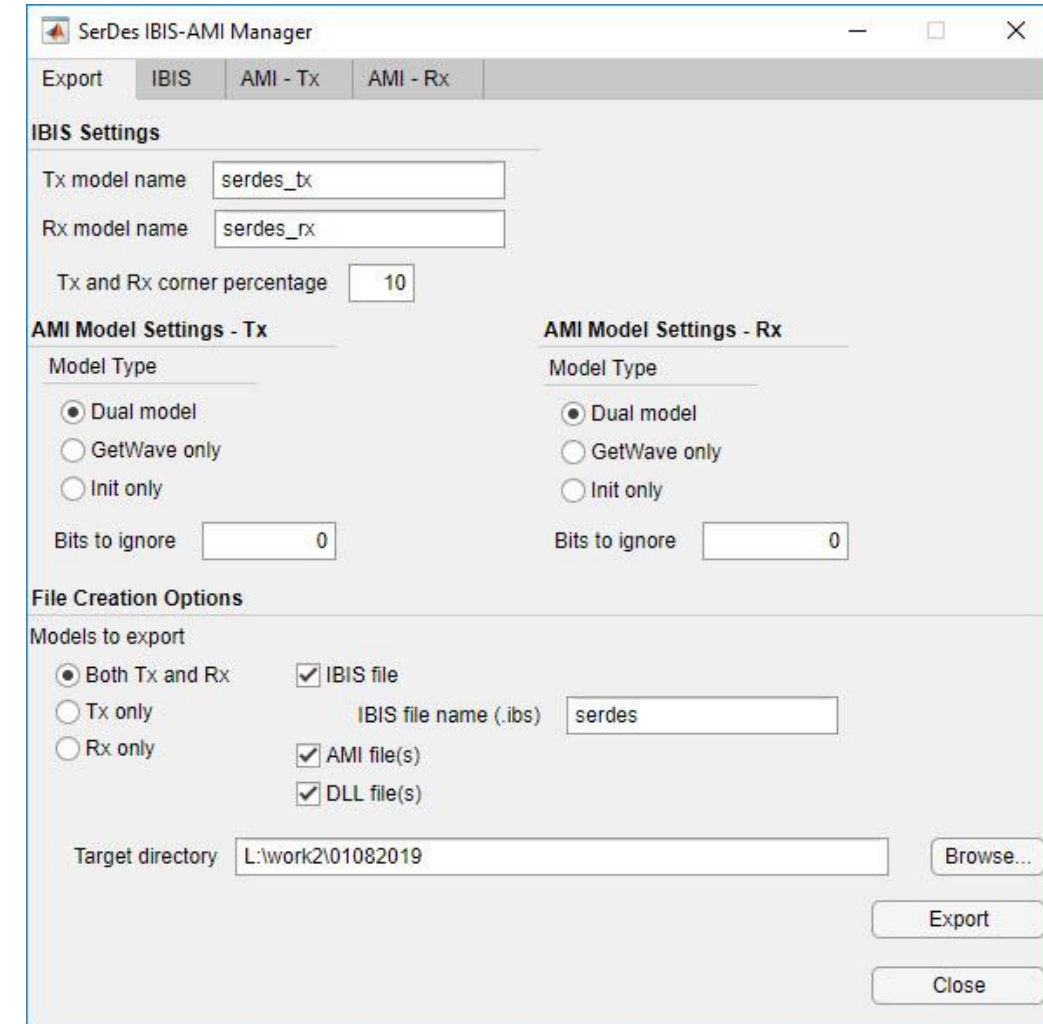
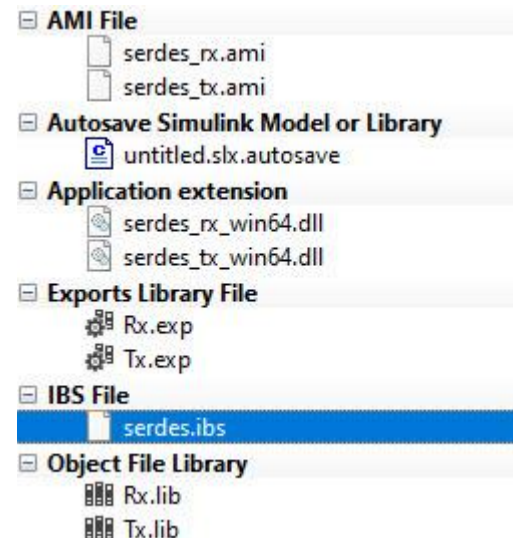


Statistical vs. Time Domain



SerDes Toolbox: IBIS-AMI Dual Model Generation

- Generate standard-compliant Init and GetWave IBIS-AMI models
- Generate associated analog IBIS model
- Customize the model interface by managing the IBIS-AMI-parameters



SerDes Verification Using Channel Simulators

Channel Simulation Using IBIS-AMI Models

- Integrate standard-compliant IBIS-AMI models in 3rd party channel simulators
 - Correlation & regression testing
 - Identification of corner cases over large families of channel models and configurations

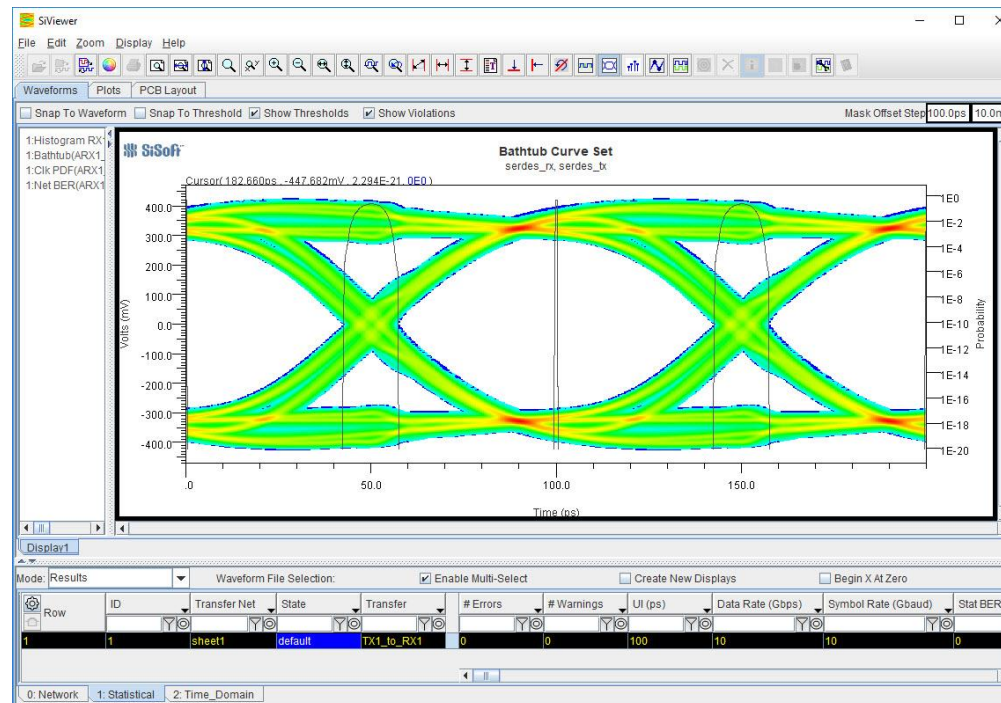
The screenshot displays the Quantum Channel Designer 300 interface. The main workspace shows a schematic diagram of a channel simulation. On the left, a transmitter model is labeled "TX1 serdes Tx serdes_tx 200.0ps - 200ps None". On the right, a receiver model is labeled "RX1 serdes Rx serdes_rx". The channel is represented by three differential pairs, labeled W1, W2, and W3, with parameters for differential strip length and length. The state is set to "default" and the topology to "sheet1".

Below the schematic is the "Solution Space" table, which lists various variables and their values for different sheets. The table has columns for Transfer Net, Variable, Type, Format, Variation Group, Value 1, and Value 2.

Transfer Net	Variable	Type	Format	Variation Group	Value 1	Value 2
sheet1	Ech	Corner	List	Corners	TE (Typ)	
sheet1	Process	Corner	List	Corners	TT (Typ)	
sheet1	RX1.CTLE.Mode	Integer	AM List	<none>	adapt	
sheet1	RX1.CTLE.ConfigSelect	Integer	AM Range	<none>	0	
sheet1	RX1.AGC.Mode	Integer	AM List	<none>	on	
sheet1	RX1.AGC.TargetRMSVoltage	Float	AM Range	<none>	0.3	
sheet1	RX1.DFECOR.ReferenceOffset	Float	AM Range	<none>	0	
sheet1	RX1.DFECOR.PhaseOffset	UI	AM List	<none>	0	
sheet1	RX1.DFECOR.Mode	Integer	AM List	<none>	adapt	
sheet1	RX1.DFECOR.TapWeights.1	Tap	AM Range	RX1.Tap	0	
sheet1	RX1.DFECOR.TapWeights.2	Tap	AM Range	RX1.Tap	0	
sheet1	RX1.DFECOR.TapWeights.3	Tap	AM Range	RX1.Tap	0	
sheet1	RX1.DFECOR.TapWeights.4	Tap	AM Range	RX1.Tap	0	
sheet1	TX1.OptmEye	String	AM List	<none>	OE	
sheet1	TX1.FFE.Mode	Integer	AM List	<none>	fixed	
sheet1	TX1.FFE.TapWeights.-1	Tap	AM Range	TX1.Tap	0	
sheet1	TX1.FFE.TapWeights.0	Tap	AM Range	TX1.Tap	1	
sheet1	TX1.FFE.TapWeights.1	Tap	AM Range	TX1.Tap	0	
sheet1	TX1.FFE.TapWeights.2	Tap	AM Range	TX1.Tap	0	

Integration with QCD/QSI (SiSoft Link)

- Bidirectional link between SerDes Toolbox and SiSoft QCD/QSI
- Automatically create a QCD/QSI project from SerDes Toolbox
- Back-annotate the channel model, stimuli, and AMI parameter settings into SerDes Toolbox
- Rapidly iterate between system design and channel simulation



Use Simulink and SerDes Toolbox

- Algorithmic design, analysis, and system-level simulation of SerDes systems with many trusted functions
- Integrate with 3rd party channel simulators for SerDes verification
 - Generate standard-compliant IBIS-AMI models
- Link with IC design tools to model implementation impairments and reuse testbenches
 - Co-simulation, HDL/SV code generation, and data post-processing

Thank You!
Q&A